CMS8S589x Datasheet

Enhanced 1T 8051 microcontroller with flash memory

Rev. 1.0.5

1. Product Features

1.1 Features

- **Compatible with MCS-51 1T instruction system**
  - The system clock frequency supports up to 48MHz
  - The maximum machine cycle supports $1T_{SYS}$ @ F_{SYS}=16MHz
  - The maximum machine cycle supports $2T_{SYS}$ @ F_{SYS}=24MHz
  - The maximum machine cycle supports $3T_{SYS}$ @ F_{SYS}=48MHz
- Memory
  - Maximum program FLASH: 64K×8Bit
  - Data FLASH: 4K×8Bit
  - Maximum Data BOOT FLASH: 16K×8Bit
  - General RAM: 256×8Bit
  - Universal XRAM: 4K×8Bit
  - Program FLASH supports partition protection
- **4 oscillation modes**
  - HSI-Internal high-speed oscillation: 48MHz
  - HSE-External high-speed oscillation: 8MHz/16MHz
  - LSE-External low-speed oscillation: 32.768KHz
  - LSI-Internal low-speed oscillation: 125KHz
- **Low voltage reset function（LVR）**
  - 1.8V/2.0V/2.5V/3.5V
- **Low-voltage detection function（LVD）**
  - 2.0V/2.2V/2.4V/2.7V/3.0V/3.7V/4.0V/4.3V
- **GPIO**
  - Up to 30 GPIOs
  - All digital functions can be assigned to any GPIO
  - Both support pull-up/down resistor function
  - Both support edge (rising edge/ falling edge/ both edge) interrupt
  - Support wake-up function
- **Interrupt source**
  - Support all external port interrupts
  - Up to 8 timer interrupts
  - Other peripheral interrupts
- **Operating voltage range**
  - 2.1V～5.5V
- **Operating temperature range**
  - -40℃～105℃
- **Communication module**
  - Up to 1xSPI (communication rate up to 6Mb/s)
  - 1xI2C (communication rate up to 400Kb/s)
  - Up to 2xUART (baud rate up to 1Mb/s)
- **Low power mode**
  - Idle mode（IDLE）
  - Sleep mode（STOP）
- **Timer**
  - WDT timer (watchdog timer)
  - Up to 5 timers: Timer0/1，Timer2，Timer3/4
  - LSE Timer (Support sleep wake function)
- **Buzzer driver**
  - 50% duty cycle, frequency can be set freely
- **Enhanced PWM**
  - 6 channels enhanced PWM
  - 6 mutually independent cycle counters
  - Support independent /complementary/ synchronous/ group mode
  - Support edge alignment/center alignment
  - Support complementary mode dead zone delay function
  - Support mask function and brake function
- **High-precision 12-bit ADC**
  - All GPIOs (30I/Os) support AD channels
  - Optional reference voltage (2.0V/2.4V/3.0V/VDD)
  - Can detect internal 1.2V reference voltage
  - Support hardware trigger start conversion function
  - Support a set of result digital comparison function
- **Support 96-bit unique ID number (UID)**
  - Each chip has an independent ID number
- **Support two-wire serial programming and debugging**

1.2 Product Comparison

Product mode / Peripheral interface		CMS8S5895	CMS8S5897	CMS8S5898	CMS8S5899
Maximum clock frequency		48 MHz			
Memory Size	APROM	64 KB			
	BOOT	2/4/8/16 KB			
	Data FLASH	4 KB			
	RAM	256 B			
	XRAM	4 KB			
Timer	WDT	1			
	WWDT	1			
	Timer0/1	2 (16bit)			
	Timer2	1 (16bit)			
	Timer3/4	2 (16bit)			
	LSE Timer	1 (16bit)			
	WUT	1 (12bit)			
	BRT	1 (16bit)			
Enhanced Digital peripherals	BUZZER	1			
	PWM	6(16bit)			
Communication module	SPI	1			
	I^2C	1			
	UART	2			
Analog module	12bit-ADC (Number of external channels)	18	18	22	30
GPIOs		18	18	22	30
LVR		1.8V/2.0V/2.5V/3.5V			
LVD		2.0V/2.2V/2.4V/2.7V/3.0V/3.7V/4.0V/4.3V			
Operating voltage		2.1~5.5 V			
Operating temperature		-40~105 ℃			
Package		SSOP20	QFN20 TSSOP20	QFN24 SSOP24	LQFP32 QFN32

2. System Overview

2.1 System Introduction

The CMS8S589x series is an 8051 core, a 1T instruction system compatible with MCS-51, and a general IO type 8-bit chip. The operating frequency can reach up to 48MHz. The MCU has the following characteristics:

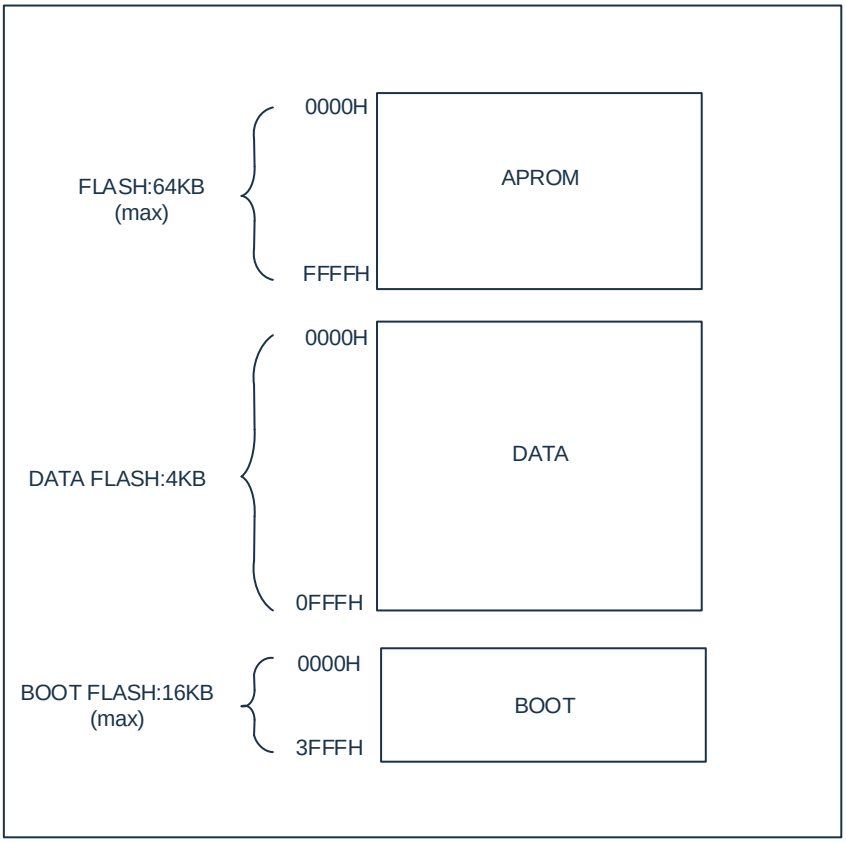
- With a maximum of 64KB program area, 256B RAM space, 4KB XRAM, 4KB DATA FLASH area, 16K BOOT area.
- With four oscillation modes.
- It supports three working modes: normal, idle, and sleep, which can effectively reduce power consumption.
- Built-in low-voltage reset LVR, low-voltage detection LVD, watchdog overflow reset and other protection settings can effectively improve the reliability of system operation.
- With multiple interrupt sources such as external interrupts, timer interrupts and other peripheral interrupts, it can respond to external events in a timely manner and improve the utilization of the MCU.
- Digital functions can be assigned to any IO port.
- 10 timers can realize functions such as reset system, counting, input capture, output comparison, timing wake-up, and baud rate generator.
- 6-channel 16-bit PWM, supports independent, complementary, and synchronous three-mode output, and has hardware brake function, dead zone control function, mask output and other functions.
- With 1 I2C, 1 SPI, and 2 UART communication modules, it can realize data transmission between the system and other devices.
- It has a high-precision 12-bit ADC and can choose an internal reference voltage; Each IO can be used as the input channel of the ADC.

2.2 Memory Structure

2.2.1 Program Memory FLASH

This series has a maximum of 84KB of FLASH storage space, The storage space is divided into three parts, namely the program area (APROM area), DATA area, BOOT area.

The block diagram of the FLASH space allocation structure is as follows:

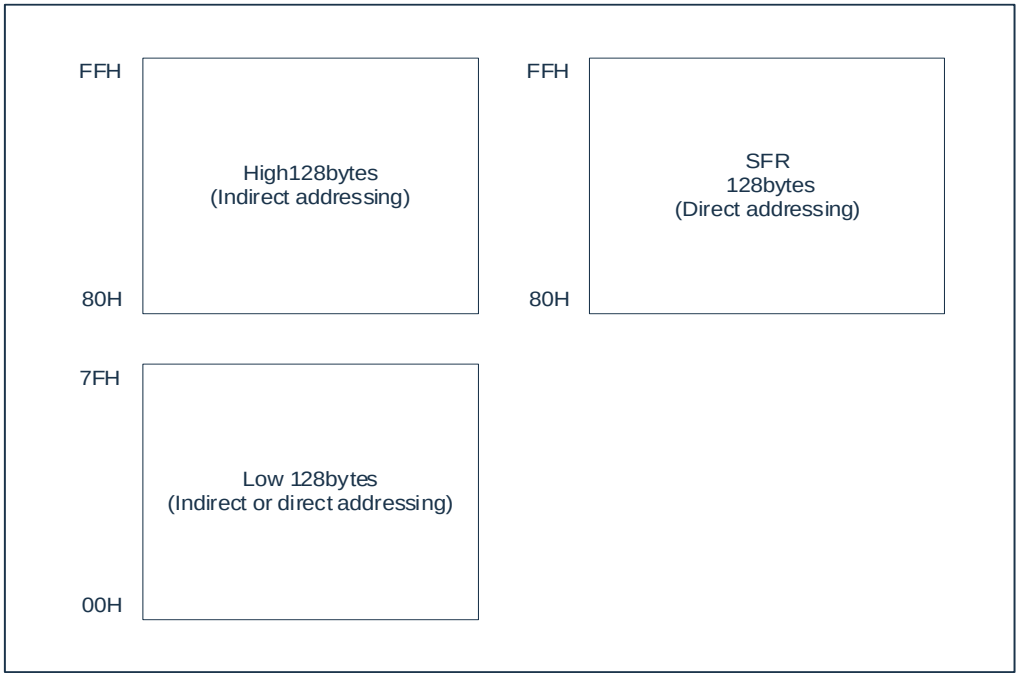


CMS8S589x can configure the size of BOOT, the configuration method is as follows:

Address space allocation method	Space size of BOOT area	BOOT area address
method0	2K	0000H-07FFH
method1	4K	0000H-0FFFH
method2	8K	0000H-1FFFH
method3	16K	0000H-3FFFH

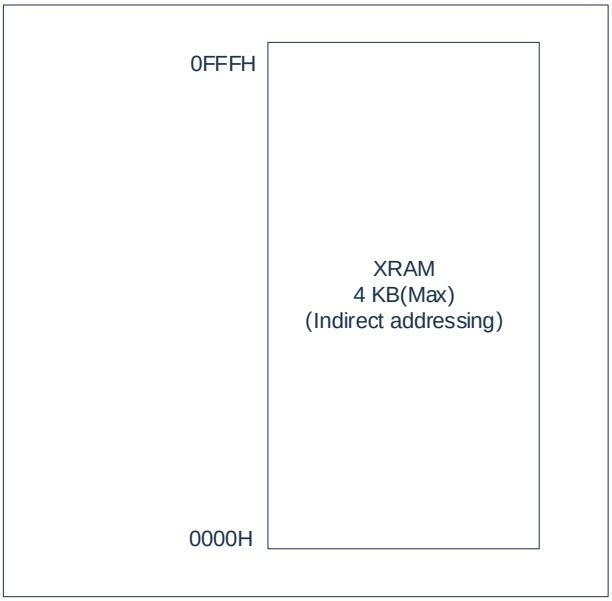
2.2.2 Internal Data Memory RAM

The internal data memory is divided into 3 parts: low 128Bytes, high 128Bytes, SFR. The structure diagram of RAM space allocation is shown in the figure below:



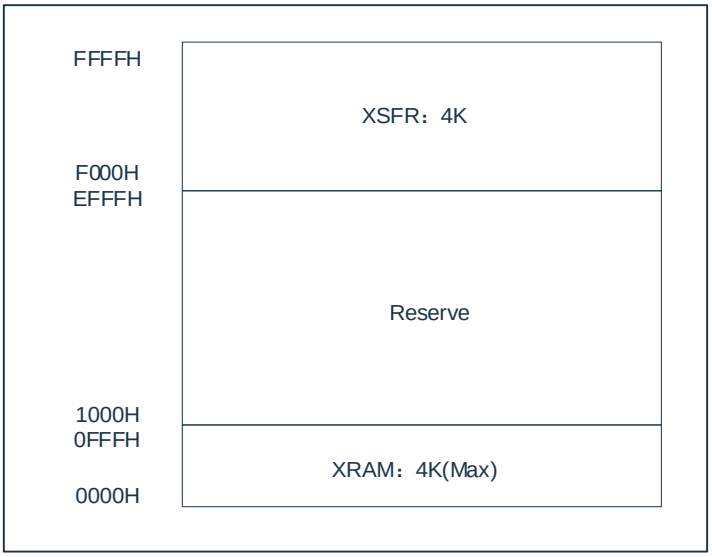
2.2.3 External Data Memory XRAM

There is a maximum 4KB XRAM area inside the chip, which is not related to RAM/FLASH. The structure diagram of XRAM space allocation is shown in the figure below.



2.2.4 Special Function Register XSFR

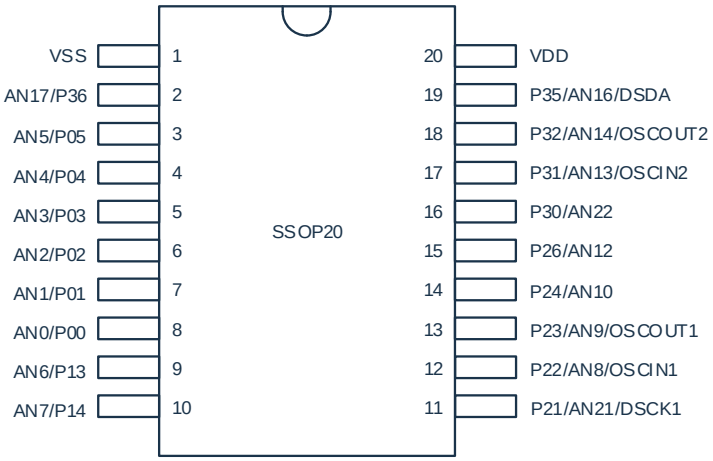
XSFR is a special register shared by the addressing space and XRAM, which mainly includes: port control register and other function control registers. Its addressing range is as follows:



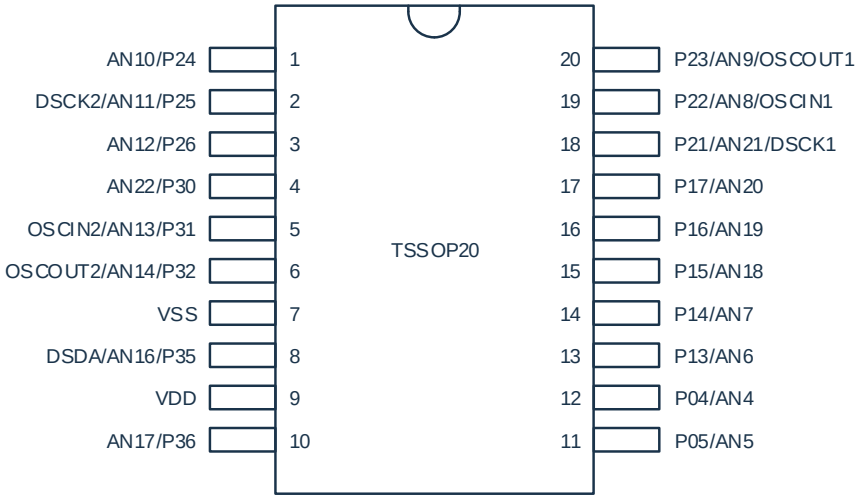
3. Pin Assignment

3.1 Pin Description

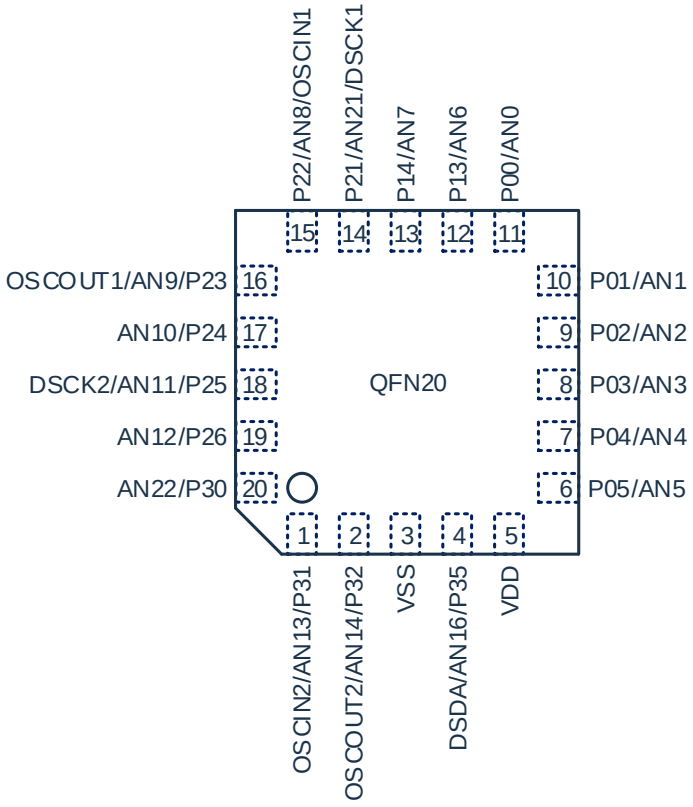
3.1.1 CMS8S5895-SSOP20 Pin Diagram



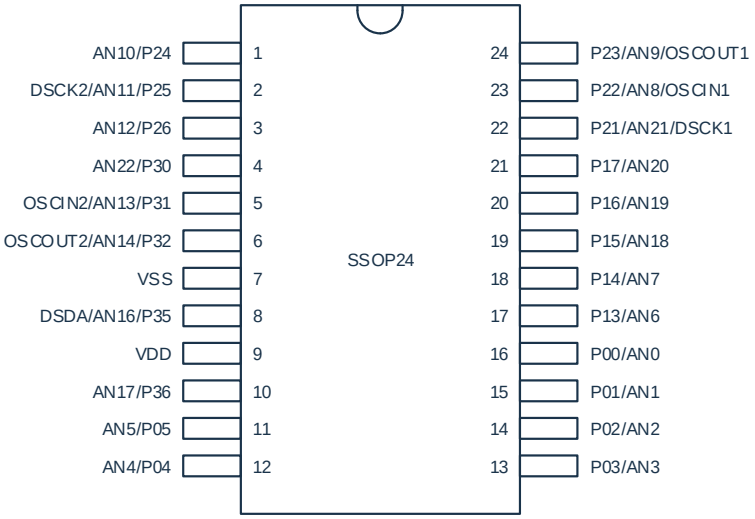
3.1.2 CMS8S5897-TSSOP20 Pin Diagram



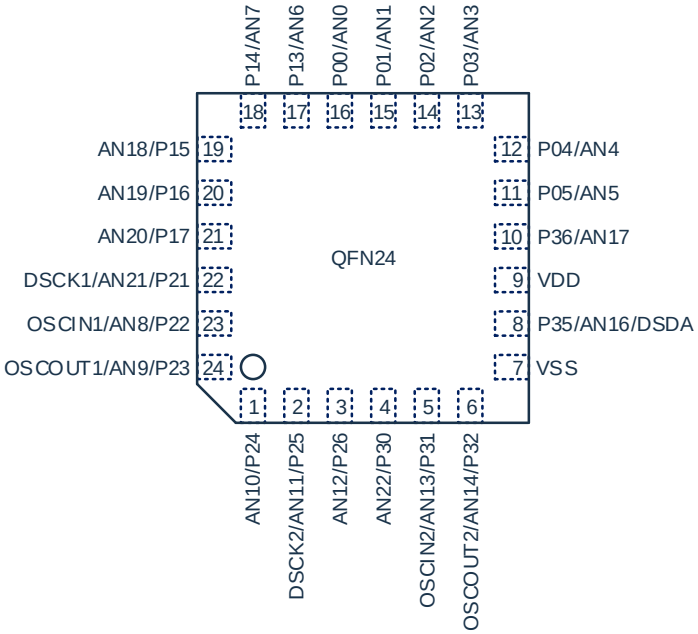
3.1.3 CMS8S5897-QFN20 Pin Diagram



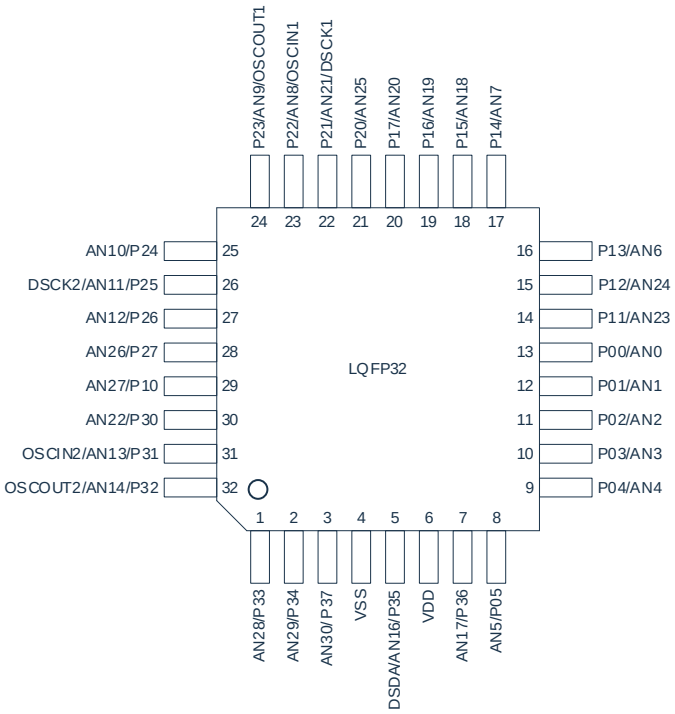
3.1.4 CMS8S5898-SSOP24 Pin Diagram



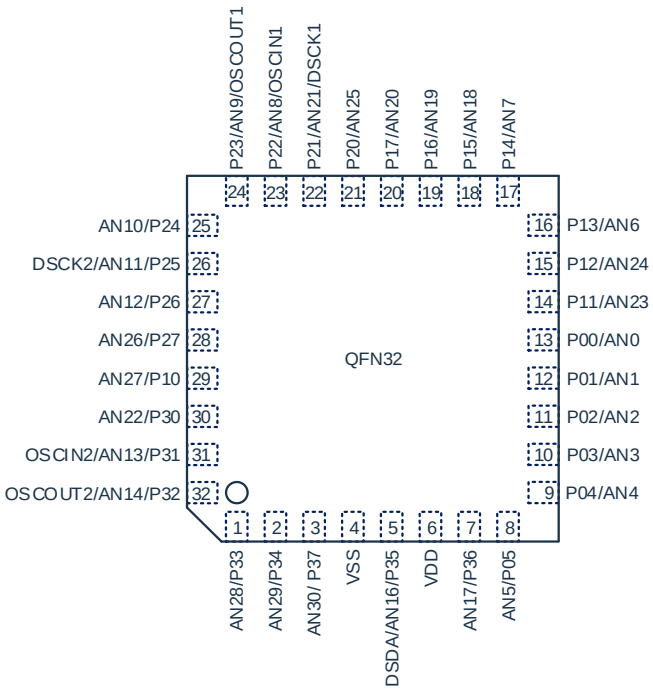
3.1.5 CMS8S5898-QFN24 Pin Diagram



3.1.6 CMS8S5899-LQFP32 Pin Diagram



3.1.7 CMS8S5899-QFN32 Pin Diagram



3.2 Pin Function Description

Pin number							Pin Function	Pin Type	Pin description
CMS8S5895	CMS8S5897		CMS8S5898		CMS8S5899				
SSOP20	TSSOP 20	QFN 20	SSOP 24	QFN 24	LQFP 32	QFN 32			
8	-	11	16	16	13	13	P00	I/O	GPIO configures input, output, pull-up, pull-down and other functions through registers
							AN0	I	ADC channel 0 input
7	-	10	15	15	12	12	P01	I/O	GPIO configures input, output, pull-up, pull-down and other functions through registers
							AN1	I	ADC channel 1 input
6	-	9	14	14	11	11	P02	I/O	GPIO configures input, output, pull-up, pull-down and other functions through registers
							AN2	I	ADC channel 2 input
5	-	8	13	13	10	10	P03	I/O	GPIO configures input, output, pull-up, pull-down and other functions through registers
							AN3	I	ADC channel 3 input
4	12	7	12	12	9	9	P04	I/O	GPIO configures input, output, pull-up, pull-down and other functions through registers
							AN4	I	ADC channel 4 input
3	11	6	11	11	8	8	P05	I/O	GPIO configures input, output, pull-up, pull-down and other functions through registers
							AN5	I	ADC channel 5 input
-	-	-	-	-	29	29	P10	I/O	GPIO configures input, output, pull-up, pull-down and other functions through registers
							AN27	I	ADC channel 27 input
-	-	-	-	-	14	14	P11	I/O	GPIO configures input, output, pull-up, pull-down and other functions through registers
							AN23	I	ADC channel 23 input
-	-	-	-	-	15	15	P12	I/O	GPIO configures input, output, pull-up, pull-down and other functions through registers
							AN24	I	ADC channel 24 input
9	13	12	17	17	16	16	P13	I/O	GPIO configures input, output, pull-up, pull-down and other functions through registers
							AN6	I	ADC channel 6 input
10	14	13	18	18	17	17	P14	I/O	GPIO configures input, output, pull-up, pull-down and other functions through registers
							AN7	I	ADC channel 7 input
-	15	-	19	19	18	18	P15	I/O	GPIO configures input, output, pull-up, pull-down and other functions through registers
							AN18	I	ADC channel 18 input
-	16	-	20	20	19	19	P16	I/O	GPIO configures input, output, pull-up, pull-down and other functions through registers
							AN19	I	ADC channel 19 input
-	17	-	21	21	20	20	P17	I/O	GPIO configures input, output, pull-up, pull-down and other functions through registers

Pin number							Pin Function	Pin Type	Pin description
CMS8S5895	CMS8S5897		CMS8S5898		CMS8S5899				
SSOP20	TSSOP 20	QFN 20	SSOP 24	QFN 24	LQFP 32	QFN 32			
							AN20	I	ADC channel 20 input
-	-	-	-	-	21	21	P20	I/O	GPIO configures input, output, pull-up, pull-down and other functions through registers
							AN25	I	ADC channel 25 input
11	18	14	22	22	22	22	P21	I/O	GPIO configures input, output, pull-up, pull-down and other functions through registers
							AN21	I	ADC channel 21 input
							DSCK1	I/O	Two-wire programming, debugging clock input and output channel 1
12	19	15	23	23	23	23	P22	I/O	GPIO configures input, output, pull-up, pull-down and other functions through registers
							AN8	I	ADC channel 8 input
							OSCIN1	I	External oscillator 1 input
13	20	16	24	24	24	24	P23	I/O	GPIO configures input, output, pull-up, pull-down and other functions through registers
							AN9	I	ADC channel 9 input
							OSCOUT 1	O	External oscillator 1 output
14	1	17	1	1	25	25	P24	I/O	GPIO configures input, output, pull-up, pull-down and other functions through registers
							AN10	I	ADC channel 10 input
-	2	18	2	2	26	26	P25	I/O	GPIO configures input, output, pull-up, pull-down and other functions through registers
							AN11	I	ADC channel 11 input
							DSCK2	I/O	Two-wire programming, debugging clock input and output channel 2
15	3	19	3	3	27	27	P26	I/O	GPIO configures input, output, pull-up, pull-down and other functions through registers
							AN12	I	ADC channel 12 input
-	-	-	-	-	28	28	P27	I/O	GPIO configures input, output, pull-up, pull-down and other functions through registers
							AN26	I	ADC channel 26 input
16	4	20	4	4	30	30	P30	I/O	GPIO configures input, output, pull-up, pull-down and other functions through registers
							AN22	I	ADC channel 22 input
17	5	1	5	5	31	31	P31	I/O	GPIO configures input, output, pull-up, pull-down and other functions through registers
							AN13	I	ADC channel 13 input
							OSCIN2	I	External oscillator 2 input
18	6	2	6	6	32	32	P32	I/O	GPIO configures input, output, pull-up, pull-down and other functions through registers
							AN14	I	ADC channel 14 input
							OSCOUT 2	O	External oscillator 2 output
-	-	-	-	-	1	1	P33	I/O	GPIO configures input, output, pull-up, pull-down and other functions through

Pin number							Pin Function	Pin Type	Pin description
CMS8S5895	CMS8S5897		CMS8S5898		CMS8S5899				
SSOP20	TSSOP 20	QFN 20	SSOP 24	QFN 24	LQFP 32	QFN 32			
									registers
							AN28	I	ADC channel 28 input
-	-	-	-	-	2	2	P34	I/O	GPIO configures input, output, pull-up, pull-down and other functions through registers
							AN29	I	ADC channel 29 input
19	8	4	8	8	5	5	P35	I/O	GPIO configures input, output, pull-up, pull-down and other functions through registers
							AN16	I	ADC channel 16 input
							DSDA	I/O	Two-wire programming, debugging clock input and output channels
2	10	-	10	10	7	7	P36	I/O	GPIO configures input, output, pull-up, pull-down and other functions through registers
							AN17	I	ADC channel 17 input
-	-	-	-	-	3	3	P37	I/O	GPIO configures input, output, pull-up, pull-down and other functions through registers
							AN30	I	ADC channel 30 input
20	9	5			6	6	VDD	P	Power supply voltage input pin
1	7	3	9	9	4	4	VSS	P	Ground pin

3.3 GPIO Features

The pins share multiple functions, and each I/O port can be configured as any digital function or designated analog function. I/O as a general GPIO port has the following characteristics:

- Configurable 2 levels of I/O output rate.
- Configurable 2 levels of I/O drive current.
- Can read data latch status or pin status.
- Configurable rising edge, falling edge, both edge trigger interrupt.
- Configurable rising edge, falling edge, both edge interrupt to wake up the chip.
- Can be configured as normal input, pull-up input, pull-down input, push-pull output, open-drain output mode.

3.4 Pin Function List

The digital functions of the CMS8S589x series chip pins can be assigned arbitrarily, that is, each I/O port can be assigned any digital function. The digital functions that can be assigned are shown in the table below:

Digital function	Direction	Function description
GPIO	I/O	General-purpose IO port, configure input, output, pull-up and pull-down functions through registers
CC0	O	Timer2 compare output channel 0
CC1	O	Timer2 compare output channel 1
CC2	O	Timer2 compare output channel 2
CC3	O	Timer2 compare output channel 3
TXD0	O	UART0 data output
RXD0	I/O	UART0 data input/synchronous mode data output
TXD1	O	UART1 data output
RXD1	I/O	UART1 data input/synchronous mode data output
SCL	I/O	I2C clock input and output
SDA	I/O	I2C data input and output
NSS	I/O	SPI slave mode chip select signal (input/output)
SCLK	I/O	SPI clock input and output
MOSI	I/O	SPI master sending and slave receiving
MISO	I/O	SPI master receiving and slave sending
PG0	O	PWM channel 0 output
PG1	O	PWM channel 1 output
PG2	O	PWM channel 2 output
PG3	O	PWM channel 3 output
PG4	O	PWM channel 4 output
PG5	O	PWM channel 5 output
BEEP	O	Buzzer drive output
INT0	I	External interrupt 0 input
INT1	I	External interrupt 1 input
T0	I	Timer0 external clock input
T0G	I	Timer0 gate control input
T1	I	Timer1 external clock input
T1G	I	Timer1 gate control input
T2	I	Timer2 external event or gate control input
T2EX	I	Timer2 falling edge auto-reload input
CAP0	I	Timer2 input capture channel 0
CAP1	I	Timer2 input capture channel 1
CAP2	I	Timer2 input capture channel 2
CAP3	I	Timer2 input capture channel 3
ADET	I	ADC external trigger input
FB	I	PWM external brake signal input

The analog function allocation of the pins is fixed, and each pin corresponds to a different analog function, and the pins are subject to the actual product. The analog function assignment is shown in the following table:

PIN	CONFIG	1(ANALOG)	Priority of other digital functions
P00	-	AN0	Highest
P01	-	AN1	
P02	-	AN2	
P03	-	AN3	
P04	-	AN4	
P05	-	AN5	
P10	-	AN27	
P11	-	AN23	
P12	-	AN24	
P13	-	AN6	
P14	-	AN7	
P15	-	AN18	
P16	-	AN19	
P17	-	AN20	
P20	-	AN25	
P21	DSCK1	AN21	
P22	OSCIN1	AN8	
P23	OSCOUT1	AN9	
P24	-	AN10	
P25	DSCK2	AN11	
P26	-	AN12	
P27		AN26	
P30	-	AN22	
P31	OSCIN2	AN13	
P32	OSCOUT2	AN14	
P33	-	AN28	
P34	-	AN29	
P35	DSDA	AN16	
P36	-	AN17	
P37	-	AN30	lowest

4. Function Summary

4.1 System Clock

The system clock selects the clock source and clock frequency division through the settings of the system configuration register and the oscillator control register. The chip clock source can be selected from the following 4 types:

- Internal high-speed oscillation HSI (48MHz).
- External high-speed oscillator HSE (8MHz/16MHz).
- External low-speed oscillator LSE (32.768KHz).
- Internal low-speed oscillation LSI (125KHz).

4.2 Reset

The reset operation is used to complete the initialization of the internal circuit of the chip, so that the system starts working from a certain state. The chip has the following reset methods:

- Power-on reset.
- External reset.
- Low voltage reset.
- CONFIG state protection reset.
- Power-on configuration monitoring reset.
- Watchdog overflow reset.
- Window watchdog reset.
- Software reset.

Any of the above reset situations requires a certain response time, and the system provides a complete reset process to ensure the smooth progress of the reset action.

4.3 Power Management

4.3.1 Operating Mode

The chip has 3 different working modes to meet the power consumption requirements of different applications.

- Normal working mode: MCU is in normal working state and peripherals are operating normally.
- Idle mode IDLE: MCU is in idle mode, CPU stops working, and peripherals are operating normally. This mode can be awakened by any interrupt.
- Sleep mode STOP: MCU is in sleep mode, CPU stops working, and peripherals stop working. This mode can be awakened by INT0/1 interrupt, external interrupt, WUT timer wakeup, LSE timer wakeup.

4.3.2 Power Supply Low Voltage Reset（LVR）

When the power supply voltage is lower than the set detection voltage, the system resets.

There are 4 options for low voltage reset: 1.8V/2.0V/2.5V/3.5V.

4.3.3 Power Supply Low-voltage Detection（LVD）

The low voltage detection circuit compares the power supply voltage with the set voltage, and if the power supply voltage is lower than the set voltage, an interrupt request signal is generated.

There are 8 options for the settable detection voltage: 2.0V/2.2V/2.4V/2.7V/3.0V/3.7V/4.0V/4.3V.

4.4 Interrupt Control

The chip has multiple interrupt sources and interrupt vectors. The user-settable interrupts include INT0/1, Timer0/1, Timer2, Timer3/4, WDT, LSE_Timer, PWM, I2C, SPI, UART0/1, P0/P1/P2/P3, ADC, LVD, WWDT, the actual number of interrupt sources varies by product.

The chip stipulates two interrupt priority levels, which can realize two-level interrupt nesting. When an interrupt has been responded, if a high-level interrupt sends a request, the latter can interrupt the former to achieve interrupt nesting.

4.5 Timer

4.5.1 WDT Timer

The watchdog timer is an on-chip timer whose clock source is provided by the system clock. The WDT overflow will generate a reset. The watchdog reset is a protection setting of the system. When the system runs to an unknown state, the watchdog can be used to reset the system, thereby avoiding the system from entering an infinite loop. The WDT timer has the following characteristics:

- 8 levels of watchdog overflow time are selectable.
- Watchdog overflow interrupt can be set.
- Watchdog overflow reset can be set.

4.5.2 WWDT Timer

Window watchdog timer is a 5-bit down-counting timer with clock source provided by LSI and selectable frequency division. By clearing the timer in the specified window, the system can be prevented from entering an infinite loop due to an error state. The timer can generate interrupts, wake up the system in sleep mode, and reset the chip. The WWDT timer has the following characteristics:

- 5 levels of window comparison time are selectable.
- Window watchdog overflow interrupt can be set.
- Window watchdog overflow reset can be set.

4.5.3 Timer Counter 0/1（Timer0/1）

Timer 0 is similar in type and structure to Timer 1, and is two 16-bit up-counting timers. Timer0 has 4 working modes, Timer1 has 3 working modes, they provide basic timing and event counting operations.

In "timer mode", the timer register is incremented every 12 or 4 system cycles when the timer clock is enabled. In the "counter mode", the timing register will increase whenever it detects a falling edge on the corresponding input pin (T0, PWM0 or T1). Timer0/1 has the following features:

- Can be used as a normal timer.
- Can be used for gated timing function.
- External counting function can be realized.
- Can be used for gated counting function.
- Counter overflow interrupt.

4.5.4 Timer Counter 2（Timer2）

Timer 2 is a 16-bit timer, which can be used for various digital signal generation and event capture, such as pulse generation, pulse width modulation, pulse width measurement, etc. Timer2 has the following characteristics:

- Can be used as a normal timer.
- Can be used for gated timing function.
- External counting function can be realized.
- With reload prohibition, overflow auto-reload, external pin falling edge auto-reload function.
- Capture can be triggered by rising edge, falling edge, both edges or writing the low byte of the capture register.
- With a comparison function, this function can generate a periodic signal and a PWM waveform with a controllable duty cycle.
- Interrupts can be generated for timer, external trigger, capture, and comparison.

4.5.5 Timer 3/4（Timer3/4）

Timer 3/4 is similar to timer 0/1 and is two 16-bit timers. Timer3 has 4 working modes, and Timer4 has 3 working modes. Compared with Timer0/1, Timer3/4 only provides timing operation.

When the timer is started, the value of the register (counter) is incremented every 12 or 4 system cycles.

4.5.6 LSE Timer

The LSE timer is a 16-bit up-counting timer with a clock source from the external low-speed clock LSE. The LSE timer has the following characteristics:

- Timing function.
- 16-bit timing value can be set.
- Can work normally in sleep mode.
- An interrupt can be generated when the count value is equal to the timer value.
- Timed interrupt can wake up idle mode/sleep mode.

4.5.7 WUT Timer

WUT wake-up timer is a 12-bit, up-counting timer used for wake-up from sleep and a clock source from the internal low-speed clock LSI. After the system enters the sleep mode, the CPU and all peripheral circuits stop working, and the internal low-speed clock LSI provides the clock for the WUT counter. WUT has the following characteristics:

- The system can be woken up regularly in sleep mode.
- Count clock can be divided by 1, 8, 32, 256.
- 12-bit timing value can be set.

4.5.8 BRT Timer

The BRT timer is a 16-bit baud rate timer whose clock source comes from the system clock. It mainly provides the clock for the UART module. BRT has the following characteristics:

- With independent control switch.
- Counting clock has 8 frequency division options.
- 16-bit up counting.

4.6 Enhanced Digital Peripherals

4.6.1 BUZZER

The buzzer driver is composed of an 8-bit counter, a clock driver, and a control register. It outputs a square wave with a duty cycle of 50%, and its frequency covers a wide range. BUZZER has the following characteristics:

- With separate enable control switch.
- A total of 4 levels of system clock divider ratios of 8, 16, 32, 64 can be set.
- Output frequency 8-bit control, can be set (1~255) x 2 frequency division output.

4.6.2 Enhanced PWM Module

The enhanced PWM module supports 6 PWM generators, and the period and duty cycle can be set independently. PWM has the following characteristics:

- Support 2 kinds of waveform output in single and continuous mode.
- Support 4 control modes: independent, complementary, synchronous and group control.
- Count clock can be divided by 1, 2, 4, 8, 16.
- Support two counting modes: edge alignment and center alignment, symmetrical and asymmetrical counting are supported in center alignment mode.
- Support mask output.
- Support dead zone programming.
- Output polarity can be set.
- Support cycle, compare up, compare down, zero interrupt.
- Support software brake, external port trigger brake, ADC comparison result trigger brake, ACMP output trigger brake.
- Support 4 kinds of brake recovery modes.

4.7 Communication Module

4.7.1 SPI Module

SPI is a fully configurable SPI master/slave device that allows users to configure the polarity and phase of the serial clock signal. SPI allows the MCU to communicate with serial peripherals, and it can also communicate between processors in a multi-host system. SPI has the following characteristics:

- Full-duplex synchronous serial data transmission.
- Support master/slave mode.
- Support multi-host system.
- System error detection.
- Support speed up to 1/4 of the system clock (F_{SYS}≤24MHz).
- Bit rate generates 1/4, 1/8, 1/16, 1/32, 1/64, 1/128, 1/256, 1/512 of the system clock.
- Support four transmission formats.
- Send/receive complete can generate interrupt.

4.7.2 I²C Module

The two-wire bidirectional serial bus controller I2C provides a simple and effective connection method for data exchange between the microprocessor and the I2C bus. The I2C module has the following characteristics:

- Support 4 working methods: master sending, master receiving, slave sending, slave receiving.
- Support 2 transmission speed modes:
  Standard (up to 100Kb/s);
  Fast （up to 400Kb/s）.
- Perform arbitration and clock synchronization.
- Support multi-host system.
- The host method supports 7-bit addressing mode and 10-bit addressing mode on the I2C bus (software support).
- The slave method supports 7-bit addressing mode on the I2C bus.
- Allows operation in a wide range of clock frequencies (built-in 8-bit timer).
- An interrupt can be generated when receiving/sending is complete.

4.7.3 UARTn Module

The UARTn module contains UART0 / UART1. UARTn has the following characteristics:

- Full-duplex serial port.
- Support synchronous mode.
- Support 8-bit asynchronous transceiver mode with variable baud rate.
- Support 9-bit asynchronous transceiver mode with variable baud rate.
- Baud rate can be generated by Timer1/Timer4/Timer2/BRT module.
- Send/receive complete can generate interrupt.

4.8 Analog Module

4.8.1 Analog to Digital Conversion（ADC）

ADC module is a 12-bit successive approximation analog-to-digital converter. The port analog input signal is connected to the input of the analog-to-digital converter after passing through the multiplexer. The analog-to-digital converter generates a 12-bit binary result according to the input analog signal and saves the result in the ADC result register. ADC has the following characteristics:

- All I/O ports can be used as external input channels of ADC.
- ADC conversion clock has 15 clock frequencies to choose from.
- ADC reference voltage can choose VDD/2.0V/2.4V/3.0V.
- Support optional sampling and hold time (4/8 T_{ADCK}).
- Support the average update result after 1/4/8/16 conversions are completed.
- Support external port edge, enhanced PWM trigger ADC conversion.
- Support ADC conversion result comparison output, comparison output can control enhanced PWM brake function.
- Support ADC conversion completion to generate interrupt.
- Support multiple conversion and accumulation results.

4.9 FLASH

FLASH memory includes program memory (APROM) and non-volatile data memory (Data FLASH), which can be accessed through related special function registers (SFR) to realize IAP function. FLASH memory supports the following operations:

- Byte read operation.
- Byte write/ Continuously write operation.
- Page erase operation.

4.10 Unique ID（UID）

Each chip has a 96-bit unique identification number, namely Unique identification. The UID has been set at the factory and cannot be modified by the user.

5. User Configuration

The system configuration register (CONFIG) is the FLASH option of the MCU's initial conditions, and the program cannot access and operate it. The following contents can be set through the system configuration register:

- Watchdog's working method.
- FLASH program area partition protection, code encryption, FLASH data area encryption status.
- Low voltage reset voltage.
- Disable or enable debug mode.
- Oscillation method, prescaler selection.
- Internal high-speed oscillator frequency division selection.
- External reset configuration, port selection.
- Sleep wake-up waiting time.

6. Electrical Parameters

(TA=25℃, Unless otherwise indicated)

6.1 Absolute Maximum Rating

symbol	parameter	min.	max.	unit
T_{ST}	Storage temperature	-55	150	℃
T_A	Operating temperature	-40	105	℃
VDD-VSS	Power supply voltage	-0.3	5.8	V
V_{IN}	Input voltage	VSS-0.3	VDD+0.3	V
I_{DD}	VDD maximum input current	-	120	mA
I_{SS}	VSS maximum output current	-	120	mA
I_{IO}	Maximum sink current of a single IO	-	50	mA
	Maximum source current of a single IO	-	40	mA
	Maximum sink current of all IOs	-	120	mA
	Maximum source current of all IOs	-	120	mA

Note: If the operating conditions of the device exceed the absolute maximum rating range, the device will be permanently damaged. Function is guaranteed only if the device operates within the limits specified in the manual. The absolute maximum rating of chips may affect the reliability of devices.

6.2 DC Electrical Characteristics

VDD-VSS=2.1～5.5V，T_A=25℃

symbol	parameter	test condition	min.	typical	max.	unit
VDD	Operating voltage	F_{SYS}=48MHz，machine cycle=3T	2.1	-	5.5	V
I_{DD}	Normal mode	VDD=5V，F_{SYS}=48MHz，all peripherals are off machine cycle=3T	-	5	-	mA
		VDD=3V，F_{SYS}=48MHz，all peripherals are off machine cycle=3T	-	5	-	mA
		VDD=5V，F_{SYS}=24MHz，all peripherals are off machine cycle=2T	-	4	-	mA
		VDD=3V，F_{SYS}=24MHz，all peripherals are off machine cycle=2T	-	4	-	mA
		VDD=5V，F_{SYS}=16MHz，all peripherals are off machine cycle=1T	-	3	-	mA
		VDD=3V，F_{SYS}=16MHz，all peripherals are off machine cycle=1T	-	3	-	mA
		VDD=5V，F_{SYS}=8MHz，all peripherals are off machine cycle=1T	-	2.5	-	mA
		VDD=3V，F_{SYS}=8MHz，all peripherals are off machine cycle=1T	-	2.5	-	mA
	IDLE mode	VDD=5V，F_{SYS}=48MHz，all peripherals are off	-	4.5	-	mA
		VDD=3V，F_{SYS}=48MHz，all peripherals are off	-	4.5	-	mA
		VDD=5V，F_{SYS}=24MHz，all peripherals are off	-	3.5	-	mA
		VDD=3V，F_{SYS}=24MHz，all peripherals are off	-	3.5	-	mA
		VDD=5V，F_{SYS}=16MHz，all peripherals are off	-	2.5	-	mA

		VDD=3V，F_{SYS}=16MHz，all peripherals are off	-	2.5	-	mA
		VDD=5V，F_{SYS}=8MHz，all peripherals are off	-	2	-	mA
		VDD=3V，F_{SYS}=8MHz，all peripherals are off	-	2	-	mA
I_{SLEEP1}	sleep current	all peripherals are off，LSE、LSE timer enable	-	20	-	uA
I_{SLEEP2}	sleep current	all peripherals are off，LSI、WUT timer enable	-	7	-	uA
I_{SLEEP3}	sleep current	all peripherals are off	-	6	-	uA
I_{LI}	Input leakage	-	-	-	0.1	uA
V_{IL}	Input low level	-	VSS	-	0.3VDD	V
V_{IH}	Input high level	-	0.7VDD	-	VDD	V
V_{OL}	Low output voltage	VDD=5V，I_{OL1}=12mA	-	-	0.4	V
		VDD=5V，I_{OL2}=7mA	-	-	0.4	V
		VDD=3V，I_{OL1}=9mA	-	-	0.4	V
		VDD=3V，I_{OL2}=5mA	-	-	0.4	V
V_{OH}	Output high voltage	VDD=5V，I_{OH1}=40mA	3.5	-	-	V
		VDD=5V，I_{OH2}=20mA	3.5	-	-	V
		VDD=3V，I_{OH1}=15mA	2.1	-	-	V
		VDD=3V，I_{OH2}=8mA	2.1	-	-	V
R_{PH}	Pull-up resistor	-	-	32	-	KΩ
R_{PL}	Pull-down resistor	-	-	32	-	KΩ

6.3 AC Electrical Parameter

6.3.1 Power-up and Power-down Operations

TA=25℃, does not include 32.768K crystal oscillator start-up time

symbol	parameter	test condition	min.	typical	max.	unit
T_{RESET}	Reset time	VDD=5V	-	18	-	ms
TVDDR	VDD rise rate	VDD=5V	20	-	-	us/V
TVDDF	VDD fall rate	VDD=5V	20	-	-	us/V

6.3.2 External Oscillator

symbol	parameter	test condition	min.	typical	max.	unit
V_{HSE}	Operating voltage	F=8/16MHz,C_{XT}=0-47pF	2.1	-	5.5	V
V_{LSE}	Operating voltage	F=32.768KHz,C_{XT}=10-22pF	2.1	-	5.5	V

6.3.3 Internal Oscillator

VDD=2.1V-5.5V

symbol	parameter	test condition	Frequency error	min.	typical	max.	unit
F_{HSI}	Internal high speed 48MHz	T_A=-40℃ to 105℃	±8%	-	48	-	MHz
F_{LSI}	Internal low speed 125KHz	T_A=25℃	±10%	-	125	-	KHz
		T_A=-40℃ to 105℃	±15%	-	125	-	KHz

6.3.4 Low Voltage Reset Electrical Parameter

symbol	parameter	min.	typical	max.	unit
V_{LVR1}	Low pressure detection threshold 1.8V	1.65	1.8	1.95	V
V_{LVR2}	Low pressure detection threshold 2.0V	1.85	2.0	2.15	V
V_{LVR3}	Low pressure detection threshold 2.5V	2.35	2.5	2.65	V
V_{LVR4}	Low pressure detection threshold 3.5V	3.35	3.5	3.65	V

6.3.5 LVD Electrical Parameter

symbol	parameter	min.	typical	max.	unit
V_{LVD1}	Low pressure detection threshold 2.0V	1.85	2.0	2.15	V
V_{LVD2}	Low pressure detection threshold 2.2V	2.05	2.2	2.35	V
V_{LVD3}	Low pressure detection threshold 2.4V	2.25	2.4	2.55	V
V_{LVD4}	Low pressure detection threshold 2.7V	2.55	2.7	2.85	V
V_{LVD5}	Low pressure detection threshold 3.0V	2.85	3.0	3.15	V
V_{LVD6}	Low pressure detection threshold 3.7V	3.55	3.7	3.85	V
V_{LVD7}	Low pressure detection threshold 4.0V	3.85	4.0	4.15	V
V_{LVD8}	Low pressure detection threshold 4.3V	4.15	4.3	4.45	V

6.4 FLASH Electrical Parameter

symbol	parameter	test condition	min.	typical	max.	unit
V_F	FLASH operating voltage	-	2.1	-	5.5	V
T_F	FLASH operating temperature	-	-40	25	105	℃
$N_{ENDURANCE}$	Number of erasing and writing	Program FLASH	20,000	-	-	Cycle
		Data FLASH	100,000	-	-	Cycle
T_{RET}	Data retention time	25℃	100	-	-	year
T_{ERASE}	Sector erase time	-	-	2.5	-	ms
T_{WRITE}	Write time	-	-	50	-	us
T_{READ}	Read time	-	-	3*Tsys	-	-
I_{DD1}	Read current	-	-	-	2.5	mA
I_{DD2}	Programming current	-	-	-	3.6	mA
I_{DD3}	Erase current	-	-	-	2	mA

6.5 Analog Characteristics

6.5.1 BANDGAP Electrical Characteristics

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
V_{BG}	Internal 1.2V	VDD=2.1~5.5V、T_A=25℃	1.188	1.2	1.212	V
		VDD=2.1~5.5V、T_A=-20℃ to 85℃	1.182	1.2	1.218	V
		VDD=2.1~5.5V、T_A=-40℃ to 105℃	1.176	1.2	1.224	V

6.5.2 ADC Electrical Characteristics

T_A=25℃

Symbol	Parameter		Min.	Typ.	Max.	Unit
V_{AVDD}	ADC operating voltage		2.5	-	5.5	V
V_{REF1}	Reference voltage 1		-	V_{AVDD}	-	V
V_{REF2}	Reference voltage 2		1.985	2.0	2.015	V
V_{REF3}	Reference voltage 3		2.385	2.4	2.415	V
V_{REF4}	Reference voltage 4		2.985	3.0	3.015	V
V_{ADI}	Input voltage		0	-	V_{REF}	V
N_R	Resolution		12			Bit
DNL	Differential nonlinearity error（V_{REF}=V_{AVDD}=5V,T_{ADCK}=0.5us）		±2			LSB
INL	Integral nonlinearity error（V_{REF}=V_{AVDD}=5V,T_{ADCK}=0.5us）		±4			LSB
T_{ADCK}	ADC clock cycle	V_{REF}=VDD=5V	0.125	-	-	us
		V_{REF} =V_{REF2}/ V_{REF3}/V_{REF4}	2	-	-	us
T_{ADC}	ADC conversion time (sampling and hold time 4 TADCK)		-	25	-	T_{ADCK}
F_S	Sampling rate（V_{REF}=V_{AVDD}=5V）		320			Ksps

6.6 EMC Characteristics

6.6.1 EFT Electrical Characteristics

symbol	parameter	test condition	max.	unit	level
V_{EFTB}	Fast transient voltage burst limits to be applied through 0.1uF(capacitance) on VDD and VSS pins to induce a functional disturbance	T_A = + 25℃, F_{SYS}=48MHz, conforms to IEC 61000-4-4	4800	V	4B

Note：The electrical fast transient (EFT) immunity performance is closely related to system design (including power supply structure, circuit design, layout, chip configuration, program structure, etc.). The EFTparameter in the above table is the result measured on the CMS internal test platform, and is not suitable for all application environments. The test data is only for reference. All aspects of system design may affect EFT performance. In applications with high EFT performance requirements, attention should be paid to avoid interference sources affecting system operation when designing. It is recommended to analyze interference paths and optimize the design to achieve the best anti-interference performance.

6.6.2 ESD Electrical Characteristics

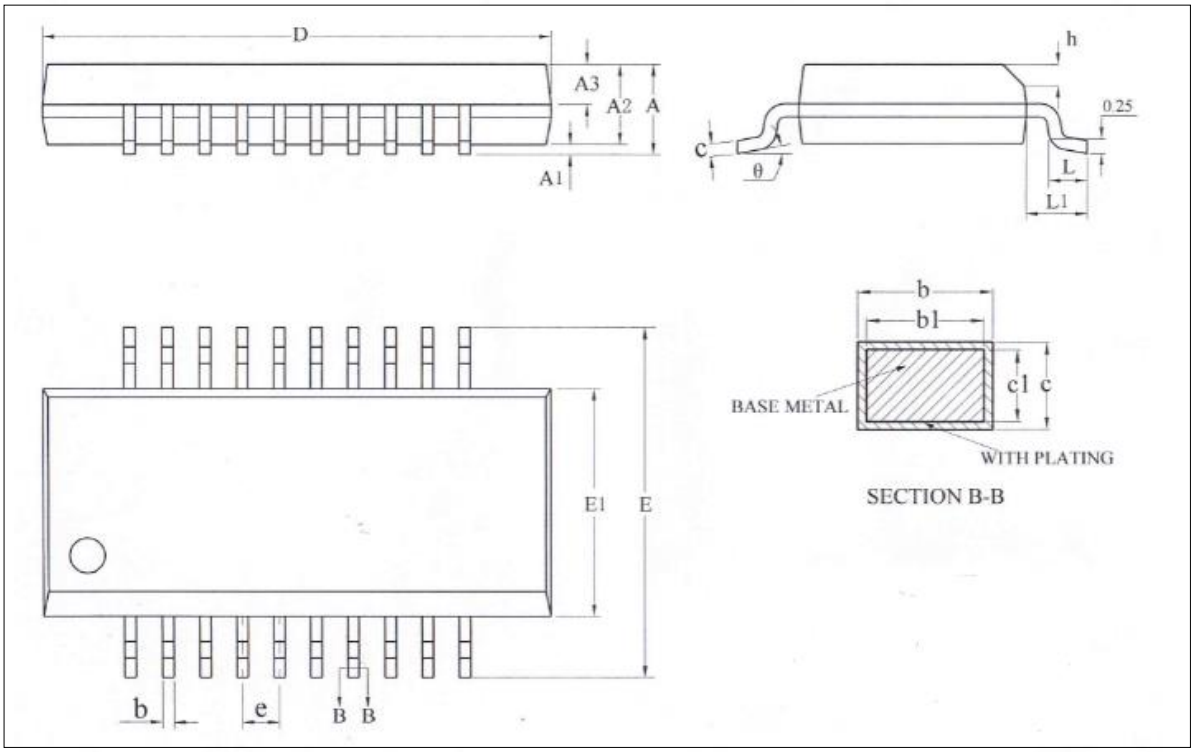
symbol	parameter	test condition	max.	unit	level
V_{ESD}	Electrostatic discharge (Human body model HBM)	T_A = + 25℃, JEDEC EIA/JESD22- A114	7500	V	3A
	Electrostatic discharge (Machine discharge mode MM)	T_A = + 25℃, JEDEC EIA/JESD22- A115	400	V	C

6.6.3 Latch-Up Electrical Characteristics

symbol	parameter	test condition	Test type	min.	unit
LU	Static latch-up class	JEDEC STANDARD NO.78E NOVEMBER 2016	Class I (T_A = +25℃)	±200	mA

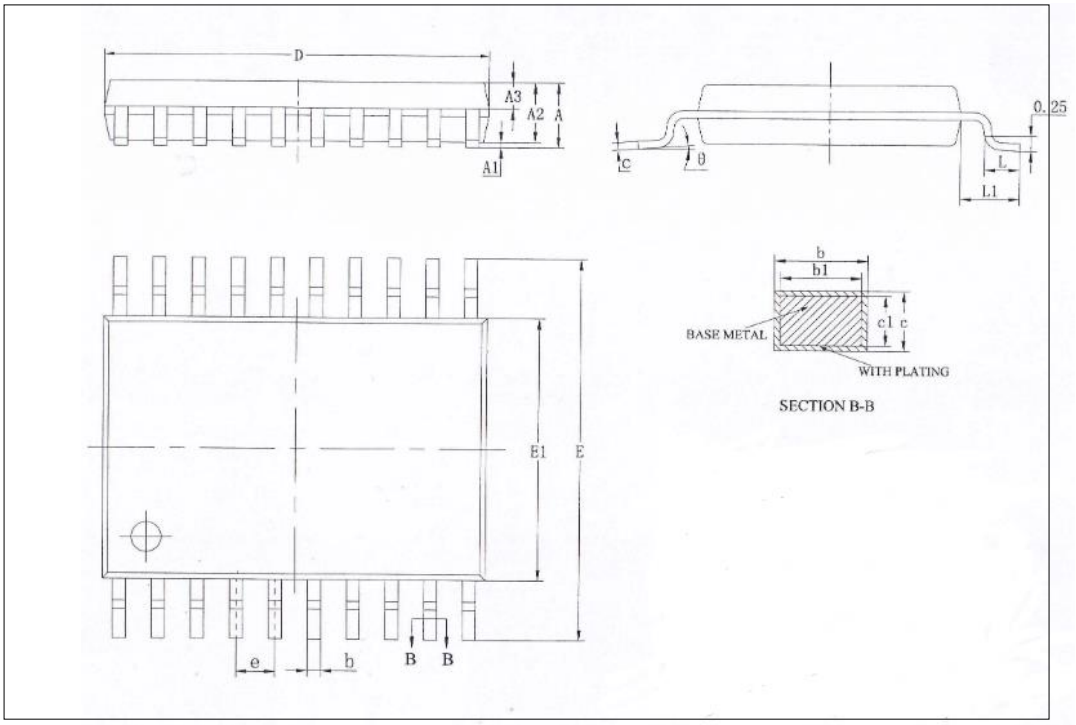
7. Package Information

7.1 SSOP20



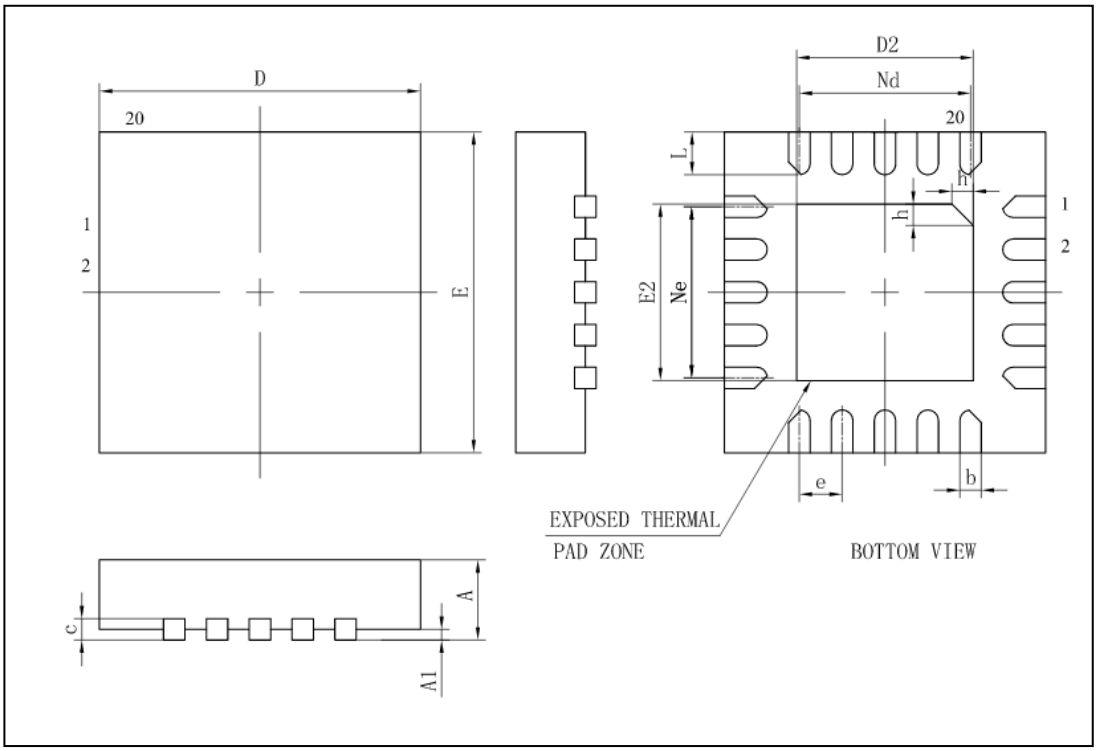
Symbol	Millimeter		
	Min	Nom	Max
A	-	-	1.75
A1	0.10	0.15	0.25
A2	1.30	1.40	1.50
A3	0.60	0.65	0.70
b	0.23	-	0.31
b1	0.22	0.25	0.28
c	0.20	-	0.24
c1	0.19	0.20	0.21
D	8.55	8.65	8.75
E	5.80	6.00	6.20
E1	3.80	3.90	4.00
e	0.635BSC		
h	0.30	-	0.50
L	0.50	0.65	0.80
L1	1.05REF		
θ	0	-	8°

7.2 TSSOP20



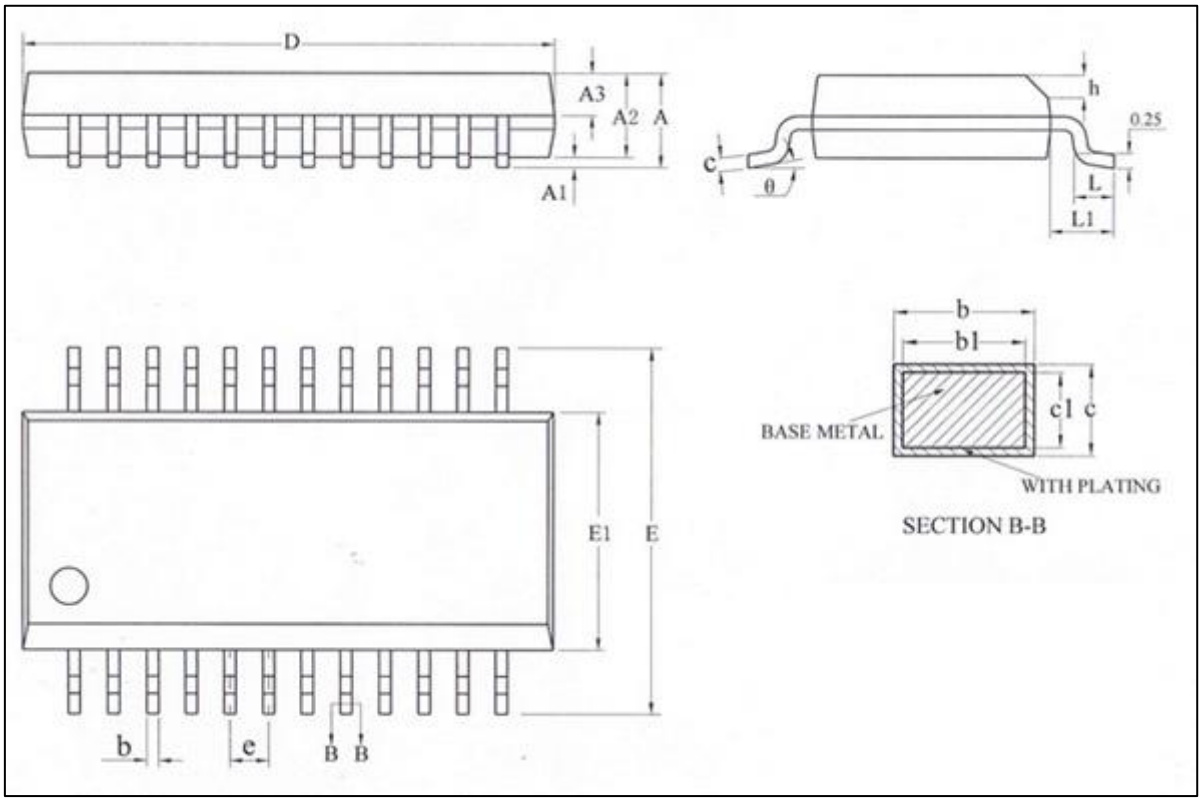
Symbol	Millimeter		
	Min	Nom	Max
A	-	-	1.20
A1	0.05	-	0.15
A2	0.80	1.00	1.05
A3	0.39	0.44	0.49
b	0.20	-	0.28
b1	0.19	0.22	0.25
c	0.13	-	0.17
c1	0.12	0.13	0.14
D	6.40	6.50	6.60
E1	4.30	4.40	4.50
E	6.20	6.40	6.60
e	0.65BSC		
L	0.45	0.60	0.75
L1	1.00REF		
θ	0	-	8°

7.3 QFN20



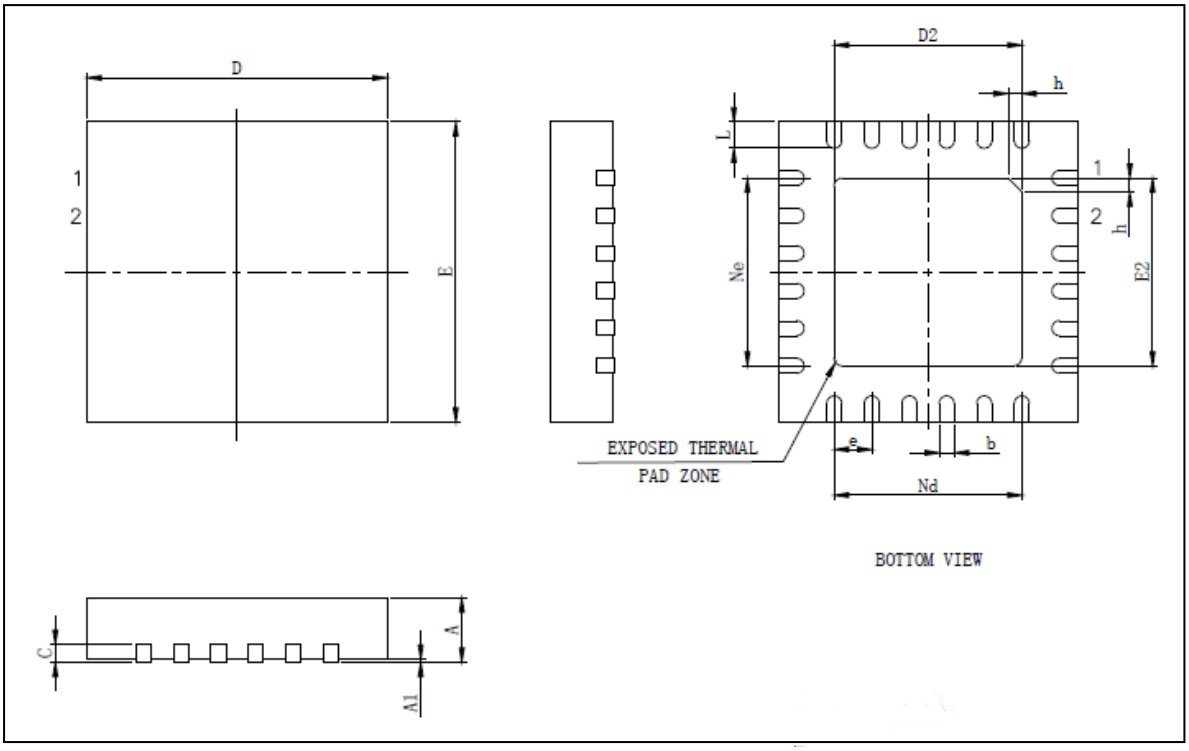
Symbol	Millimeter		
	Min	Nom	Max
A	0.70	0.75	0.80
A1	-	0.02	0.05
b	0.15	0.20	0.25
c	0.18	0.20	0.25
D	2.90	3.00	3.10
D2	1.55	1.65	1.75
e	0.4BSC		
Ne	1.6BSC		
Nd	1.6BSC		
E	2.90	3.00	3.10
E2	1.55	1.65	1.75
L	0.35	0.40	0.45
h	0.20	0.25	0.30

7.4 SSOP24



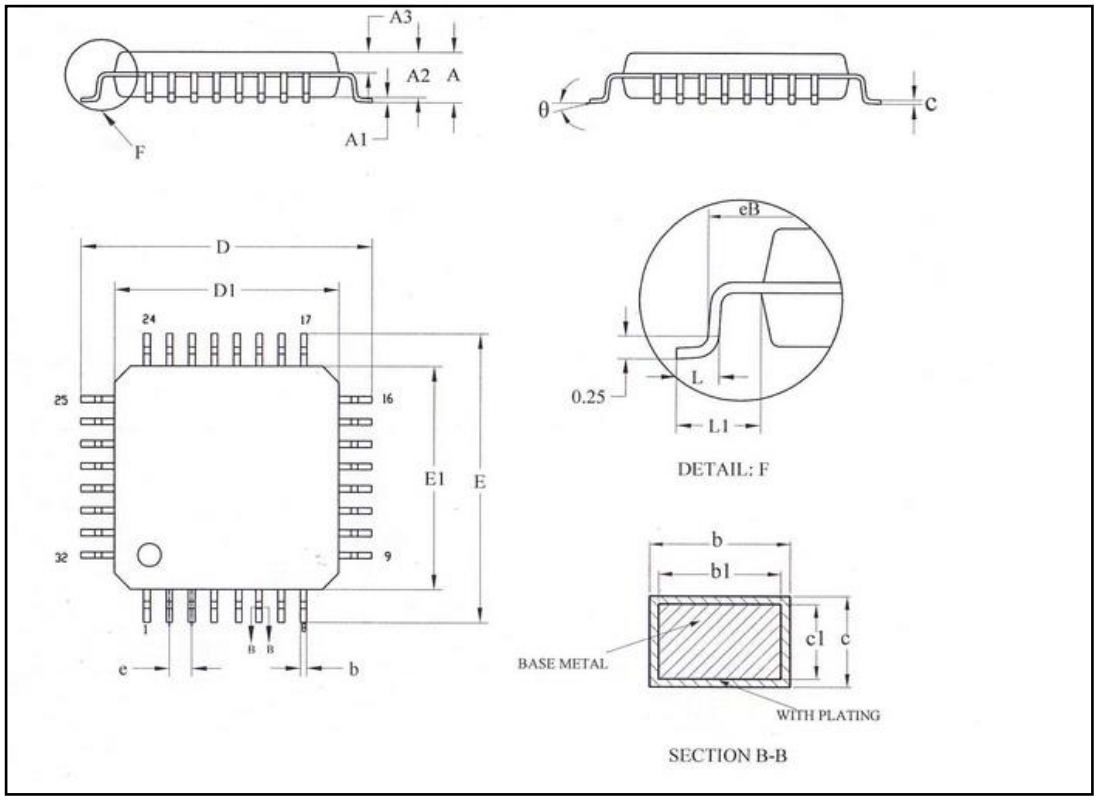
Symbol	Millimeter		
	Min	Nom	Max
A	-	-	1.75
A1	0.10	0.15	0.25
A2	1.30	1.40	1.50
A3	0.60	0.65	0.70
b	0.23	-	0.31
b1	0.22	0.25	0.28
c	0.20	-	0.24
c1	0.19	0.20	0.21
D	8.55	8.65	8.75
E	5.80	6.00	6.20
E1	3.80	3.90	4.00
e	0.635BSC		
h	0.30	-	0.50
L	0.50	-	0.80
L1	1.05REF		
θ	0	-	8°

7.5 QFN24



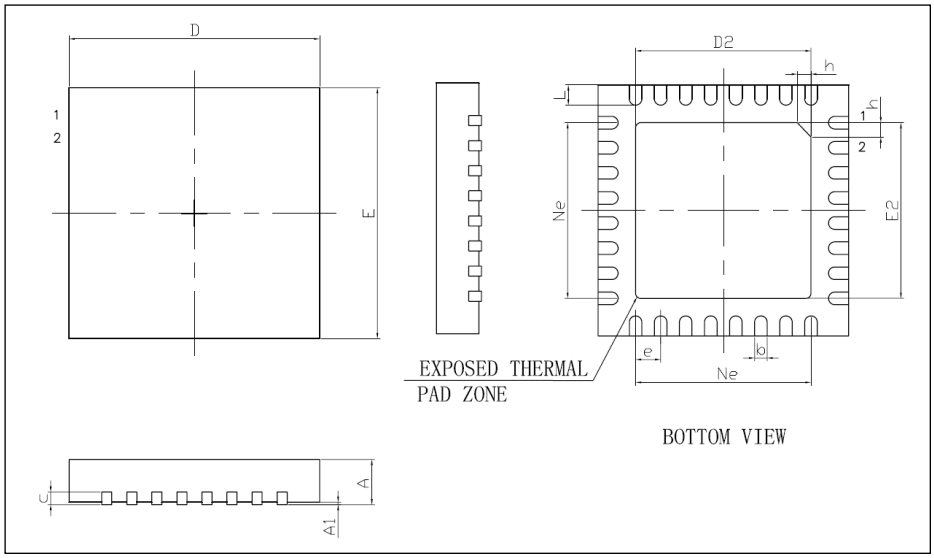
Symbol	Millimeter		
	Min	Nom	Max
A	0.70	0.75	0.80
A1	-	0.02	0.05
b	0.18	0.25	0.30
c	0.18	0.20	0.25
D	3.90	4.00	4.10
D2	2.40	2.50	2.60
e	0.50BSC		
Ne	2.50BSC		
Nd	2.50BSC		
E	3.90	4.00	4.10
E2	2.40	2.50	2.60
L	0.35	0.40	0.45
h	0.30	0.35	0.40

7.6 LQFP32



Symbol	Millimeter		
	Min	Nom	Max
A	-	-	1.60
A1	0.05	-	0.15
A2	1.35	1.40	1.45
A3	0.59	0.64	0.69
b	0.33	-	0.41
b1	0.32	0.35	0.38
c	0.13	-	0.17
c1	0.12	0.13	0.14
D	8.80	9.00	9.20
D1	6.90	7.00	7.10
E	8.80	9.00	9.20
E1	6.90	7.00	7.10
eB	8.10	-	8.25
e	0.80BSC		
L	0.45	-	0.75
L1	1.00REF		
θ	0°	-	7°

7.7 QFN32



Symbol	Millimeter		
	Min	Nom	Max
A	0.70	0.75	0.80
A1	-	0.02	0.05
b	0.18	0.25	0.30
c	0.18	0.20	0.25
D	4.90	5.00	5.10
D2	3.40	3.50	3.60
e	0.5BSC		
Ne	3.5BSC		
E	4.90	5.00	5.10
E2	3.40	3.50	3.60
L	0.35	0.40	0.45
h	0.30	0.35	0.40

8. Revision History

Revision	Date	Modify content
V1.00	Feb 2021	Initial verison
V1.01	Nov 2021	Add CMS8S5895 MCU related information
V1.02	Jan 2022	Update FLASH electrical parameter
V1.03	Feb 2022	Adjust the internal oscillator frequency error range
V1.04	Mar 2022	Adjust the internal low speed oscillator frequency error range
V1.0.5	Jul 2022	6.3.1 Power-up and Power-down Operations、 6.5.1 BANDGAP Electrical Characteristics、 6.5.2 ADC Electrical Characteristics：adjust parameters